**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

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| **Serial No.** | **09/836,884** |
| **Confirmation No.** | **5188** |
| **Application of:** | **Denis et al.** |
| **Filed:** | **April 17, 2001** |
| **Group Art Unit:** | **2823** |
| **Examiner:** | **Nguyen, K.D.** |
| **Attorney Docket No.:** | **H-303** |
| **Customer No.:** | **26245** |

Cambridge, Massachusetts
March 2, 2004

# BRIEF ON APPEAL



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Sir:

This is an appeal from the final rejection of claims 1-25, all claims pending in this application, in the Office Action issued July 29, 2003. A Notice of Appeal was filed by facsimile on October 29, 2003 (please see the Conditional Petition to Accord Date of Facsimile Transmission as Date of Filing filed herewith).

A three-month extension of time up to and including March 29, 2004, for filing an Appeal Brief is respectfully requested under 37 C.F.R. 1.136(a)(1)(ii). A Petition for Extension of Time and appropriate fee are being submitted concurrently. Also submitted with this Brief is an Appendix presenting the claims on appeal. The Appeal Brief and Appendix are submitted in triplicate in accordance with 37 C.F.R. 1.192(a).

## REAL PARTY IN INTEREST

The real party in interest in the above-identified patent application is E Ink Corporation. An Assignment perfecting E Ink Corporation's interest in this application

was recorded by the U.S. Patent and Trademark Office on August 9, 2001 at Reel 11834, Frames 0985-0994.

## RELATED APPEALS AND INTERFERENCES

Although E Ink Corporation has other appeals pending before the Board, none of them can be considered related to the present appeal.

## STATUS OF CLAIMS

Claims 1-25 are pending in this application. Claims 1-33 were originally filed, but claims 26-33 were cancelled in the Amendment dated April 28, 2003 in response to an election requirement.

Claims 1-25 stand rejected under 35 USC 103(a) as unpatentable over Noguchi (U.S. Patent No. 6,461,901) in view of the Derwent Abstract of Japanese Patent No. 63-084089, hereinafter for convenience simply referred to as "the Abstract".

The claims on appeal appear in the Appendix attached hereto.

## STATUS OF AMENDMENTS

There appears to be no doubt about the status of any papers filed in this application. The only documents filed by the applicants in response to Office Actions are a "Response to Office Action" dated September 9, 2002 electing Group I, claims 1-25, and the aforementioned Amendment dated April 28, 2003. The former paper was acknowledged by the Examiner in the Office Action of October 28, 2002, while the latter was indicated as entered in the final Office Action of July 29, 2003. No Amendment has been filed subsequent to this final Office Action.

## SUMMARY OF INVENTION

This invention relates to a process for fabricating a transistor, typically a thin film transistor, on a substrate.

Thin film transistors (TFT's) are known to be useful for, inter alia, controlling various types of display; for example TFT's are commonly used to control

liquid crystal displays used in portable computers and similar electronic devices. TFT's can also be used to control electrophoretic displays.

Although most TFT's have previously been fabricated on rigid substrates, there is increasing interest in fabricating TFT's on flexible substrates, especially flexible polymeric films. TFT's fabricated on such flexible substrates could form the basis for large displays which would be light-weight yet rugged, thus permitting their use in mobile devices. TFT's based upon amorphous silicon semiconductors are attractive for use on such flexible substrates since they allow fabrication with a minimum number of process steps and with a low thermal budget. Amorphous silicon transistors have been fabricated on ultra-thin stainless steel substrates (see, for example, Ma et al., Applied Physics Letters, 74(18), 2661 (1999)) and on polyimide films (see Gleskova et al., IEEE Electron Device Letters, 20(9), 473 (1999)).

However, the polyimide used in the process described in the latter paper, sold commercially under the name "Kapton" (Registered Trade Mark) has a glass transition temperature of only about 300°C, which restricts the temperatures which can be employed during the fabrication process, and results in a less satisfactory amorphous silicon semiconductor layer. This polyimide also has a high moisture absorption (about 4 percent by weight) and such high moisture absorption can result in swelling of the substrate and consequent cracking of thin layers deposited on the substrate, or delamination of thin layers from the substrate. Although stainless steel substrates can withstand process temperatures much higher than 300°C, such substrates require both passivation and planarization steps before transistors can be fabricated thereon. Passivation is required to ensure proper electrical isolation between adjoining metal conductors to be formed on the substrate, and to ensure that potential contaminants within the stainless steel do not diffuse into the transistors. Stainless steel substrates do, however, have the advantages of high dimensional stability and ease of handling in a manufacturing environment.

The present invention is based upon the discovery that certain types of polyimides possess properties which render them very suitable for use as substrates in the fabrication of TFT's. These polyimide substrates may be used with or without a metal backing layer.

Accordingly, this invention provides a process for forming at least one transistor on a substrate by depositing on the substrate at least one layer of semiconductor material. In the present process, the substrate comprises a polyphenylene polyimide. This process is especially intended for the formation of amorphous silicon transistors.

## ISSUES

The appellants believe that the sole issue to be decided in this appeal is whether claims 1-25 are unpatentable under 35 USC 103(a) over Noguchi, U.S. Patent No. 6,461,901, in view of the Derwent Abstract of Japanese Patent Application 63084089.

The Examiner's statement of this rejection in the Final Office Action is as follows:

Noguchi teaches a process for forming at least one transistor on a substrate 100, the process comprises depositing on the substrate at least one layer of semiconductor material (amorphous silicon) 104 by plasma enhanced chemical vapor deposition wherein the semiconductor material is affected on a continuous web of substrate (col. 10, lines 9-40 and FIGS. 10A-C). The process further comprising:

depositing a metal layer (chromium (Cr)) 102 upon the substrate on the same side thereof as the semiconductor material wherein the metal layer is deposited as a continuous film and is thereafter patterned prior to deposition of the semiconductor material thereon (col. 15, lines 46-51);

depositing a dielectric layer (silicon nitride) 103 over the metal layer by plasma enhanced chemical vapor deposition prior to the deposition of the semiconductor layer; and,

depositing a n-type silicon layer 105 over the amorphous silicon layer where in a patterned layer of metal 107 has walls defining apertures extending through the metal layer is thereafter formed over the n-type silicon, and the resultant structure is thereafter etched to remove portions of the n-type silicon not covered by the patterned layer of metal.

Noguchi discloses in FIG. 1 that the amorphous silicon 1104 is not patterned so that it extends continuously between at least some pairs of adjacent transistors as recited in present claim 20 by the applicants.

Noguchi also discloses in (col. 22, lines 14-43) wherein the deposition of the semiconductor material is effected at a temperature in excess of about 300°C as recited in present claim 13 by the applicants.

Noguchi fails to teach that the substrate comprises a polyphenylene polyimide wherein the polyphenylene polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and wherein the substrate is heated to a temperature greater than about 150°C for a period of at least about 1 minute or to a temperature greater than about 250°C for a period of at least 1 hour before deposition of the passivating layer and wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 5 hours after deposition of the passivating layer as recited in present claims 1-3, 8-10.

(JP 63084089) teaches producing a substrate comprises 3,3',4,4' biphenyl tetracarboxylic acid wherein the substrate is heated to a temperature from 100°C-300°C in at least 0.5 hour before the deposition of any other layer thereto (See the Abstract). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate (JP 63084089)'s teaching into Noguchi's method because in doing so a substrate has excellent heat resistance, cold resistance, mechanical property, electric property, wear resistance, chemical resistance and curling resistance can be obtained (See the Abstract).

Noguchi fails to teach wherein a passivating layer comprises silicon dioxide or aluminum nitride having a thickness in the range of about 20 to about 100 nm is deposited on both surfaces of the substrate before the semiconductor material is deposited thereon as recited in present claims 4-7. However, it is well-known to one of ordinary skill in the art of making semiconductor devices to deposit a passivating layer comprises silicon dioxide or aluminum nitride having a desired thickness on both surfaces of the substrate before the semiconductor material is deposited thereon.

Noguchi teaches that the substrate is being heated for the time duration but fails to teach the ranges for the time duration as recited in present claims 8-10. However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for the time duration through routine experimentation and optimization to obtain optimal or desired device performance because the time duration is result-effective variables and there is no evidence indicating that the time duration is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Although appellants believe that the above-identified two issues correspond to all of the pending rejections, *ex abundam cautelam* appellants also appeal any other bases for rejection of the pending claims which were not explicitly stated in the final Office Action, but which may be regarded as still pending.

## GROUPING OF CLAIMS

The rejected claims 1-25 do not stand or fall together.

Claims 1-11 and 13-25 stand or fall together.

For reasons discussed below, claim 12 stands alone.

## APPELLANTS' ARGUMENT

The 35 USC 103(a) rejection of claim 1, set forth in detail above, may be summarized by saying that that Noguchi teaches a process for forming at least one

transistor on a substrate, but fails to teach a substrate comprising a polyphenylene polyimide as required by all the present claims, while the Abstract teaches a substrate comprising such a polyphenylene polyimide, and that it would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of the Abstract into Noguchi's method because in doing so a substrate [that] has excellent heat resistance, cold resistance, mechanical property, electric property, wear resistance, chemical resistance and curling resistance can be obtained.

As a preliminary matter, the appellants do not dispute that Noguchi teaches a process for forming at least one thin film transistor on a substrate, but note that in Noguchi the substrate 100 is made of a quartz glass (see column 9, lines 37-38 of Noguchi). There is no discussion in Noguchi of alternative types of substrate. In the final Office Action (see the paragraph bridging pages 5 and 6), the Examiner has alleged that Noguchi does in fact disclose a substrate (FIG. 10B, 100) comprising a metal layer (FIG. 10B, 107) wherein the metal layer has walls defining apertures extending through the metal layer (column 10, lines 9-40 and FIGS. 10A-C). With respect, this reading of Noguchi is in error. Column 9, line 54 and several other points in columns 9 and 10 of Noguchi identify integer 107 in Figures 10A-10C as a source electrode. Hence, the source electrode 107 is a component of the transistor, not part of the substrate in Noguchi, and Noguchi discloses no substrate other than quartz glass.

The fact that Noguchi discloses only quartz glass as a substrate has two implications. Firstly, quartz glass is a rigid substrate, so Noguchi is an unlikely starting point for anyone wishing to approach the problem which the present invention is designed to solve, namely forming transistors on flexible substrates in order to permit the manufacture of flexible displays, as discussed above. Secondly, Noguchi does not teach any type of polymeric substrate, so that the application of the Abstract's alleged teaching to Noguchi, as proposed by the Examiner, would involve a drastic change in the Noguchi substrate, from a rigid quartz glass to a polymeric substrate.

The Abstract teaches a substrate comprising a layer of polyphenylene polyimide and a layer of metal, similar to the preferred substrate used in the present invention. However, the Abstract does not teach that this substrate is useful for the formation of film transistors thereon; the Abstract teaches only that this substrate is useful as a substrate for formation of flexible printed circuits. It will readily be apparent to anyone skilled in the art of circuit fabrication that the requirements for substrates for flexible printed circuits and substrates for formation of thin film transistors are very different from each other. Printed circuits are typically formed either by printing patterns of conductive ink on the substrate or by metallizing the substrate and patterning the resultant metal layer to form conductors. In contrast, formation of thin film transistors requires at least deposition of a gate dielectric, typically silicon nitride, and a semiconductor layer, typically amorphous silicon, and as discussed in the "Summary of Invention" section above, it is desirable that these layers be deposited at high temperatures to ensure the optimum performance from the transistor; note that in the preferred embodiment of the present invention described on page 9 of this application, the maximum processing temperature employed is 350°C (see page 9, line 16). In view of these substantial differences between the conditions required for the formation of printed circuits and thin film transistors, it would not apparent to one of ordinary skill in the relevant art whether the polyimide/metal flexible substrate taught by the Abstract could be used in the Noguchi process.

While the Abstract does state that the polyimide substrate it provides has "excellent heat resistance", this qualitative phrase must be construed with regard to the purpose for which the substrate is intended to be used, and as discussed above, the conditions typically used to form printed circuits typically do not require greatly elevated temperatures. Although the Examiner notes that the Abstract teaches that the substrate may be heated to a temperature from 100-300°C for at least 0.5 hour before the deposition of any other layer thereon, this refers to a so-called "pre-baking" of the

polyimide to remove water absorption and increase dimensional stability thereof; cf. page 6, line 22 to page 7, line 2 of this application, where a similar pre-baking step is described. This portion of the Abstract does not state what temperatures are actually used during the formation of printed circuits. Furthermore, the present application already acknowledges prior art which describes polyimides having glass transition temperatures of about 300°C (see page 1, line 24 to page 2, line 5 of the present application) so that this reference in the Abstract to use of a temperature from 100-300°C for at least 0.5 hour would not teach a person skilled in the part that the polyimide disclosed in the Abstract would have any advantage over other polyimides already known to be useful as substrates for thin film transistors.

Both the Abstract and Noguchi tacitly acknowledge differences between the substrates used for printed circuits and those used for thin film transistor arrays. As already noted, the Abstract states that its polyimide/metal flexible substrate is suitable for use in flexible printed circuits but makes no mention of suitability for use as a substrate for thin film transistor arrays. Given the relative costs per unit area of printed circuits and thin film transistor array devices (for example, backplanes for liquid crystal displays), there would appear to be every incentive for the inventors of the Abstract to claim that their substrate would be useful as a substrate for thin film transistor arrays if such a claim could plausibly be made on the basis of its suitability as a substrate for printed circuits. Furthermore, Noguchi, as already noted, forms his thin film transistors on quartz glass, a material which is not, to the best of the undersigned's knowledge, used as a substrate for printed circuits, presumably because its lack of flexibility and brittleness render it disadvantageous for the purpose. Thus, the references used in support of the 103 rejection themselves indicate that the art recognizes a clear distinction between substrates used for printed circuits and those used for thin film transistor arrays, and that a substrate used for the former is not necessarily (or even probably) useful as a substrate for the latter.

The foregoing arguments are applicable to all of claims 1-25. However, there is an additional reason why claim 12 is patentable over the references of record. Claim 12 is directed to according to claim 1 wherein the substrate comprises a metal layer on the side thereof remote from the semiconductor material, and the metal layer has walls defining apertures extending through the metal layer. As explained at page 5, lines 5-7 of this application, when the polyimide substrate is provided with a metal backing layer, this metal backing layer need not be continuous but may have apertures extending therethrough in order to reduce its stiffness and thus give the metal-backed substrate more flexibility. Neither Noguchi nor the Abstract disclose the use of a metal layer having apertures extending therethrough, and hence claim 12 cannot be obvious over these references.

## CONCLUSION

For all the foregoing reasons, the 35 USC 103(a) of all claims should be reversed and the application allowed.

A Fee Transmittal authorizing charging of the fee for the filing of this Brief on Appeal, as well as the fee for the three-month extension of time are submitted herewith. Appellants believe that the present filing necessitates no other fees. However, if any additional fees are due, the Commissioner is hereby authorized to charge any such fees to the assignee's Deposit Account No. 501162.

Respectfully submitted,

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## APPENDIX

1. A process for forming at least one transistor on a substrate, which process comprises depositing on the substrate at least one layer of semiconductor material, wherein the substrate comprises a polyphenylene polyimide.

2. A process according to claim 1 wherein the polyphenylene polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.

3. A process according to claim 2 wherein the polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine.

4. A process according to claim 1 wherein a passivating layer is deposited on the substrate before the semiconductor material is deposited thereon.

5. A process according to claim 4 wherein the passivating layer comprises silicon dioxide or aluminum nitride.

6. A process according to claim 4 wherein the passivating layer has a thickness in the range of about 20 to about 100 nm.

7. A process according to claim 4 wherein the passivating layer is deposited on both surfaces of the substrate.

8. A process according to claim 4 wherein the substrate is heated to a temperature greater than about 150°C for a period of at least about 1 minute before deposition of the passivating layer.

9. A process according to claim 4 wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 5 hours after deposition of the passivating layer.

10. A process according to claim 1 wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 1 hour before deposition of the semiconductor material.

11. A process according to claim 1 wherein the substrate comprises a metal layer on the side thereof remote from the semiconductor material.

12. A process according to claim 11 wherein the metal layer has walls defining apertures extending through the metal layer.

13. A process according to claim 1 wherein the deposition of the semiconductor material is effected at a temperature in excess of about 300°C.

14. A process according to claim 1 wherein a metal layer is deposited upon the substrate on the same side thereof as the semiconductor material but prior to the deposition of the semiconductor material.

15. A process according to claim 14 wherein the metal layer comprises chromium.

16. A process according to claim 14 wherein the metal layer is deposited as a continuous film and is thereafter patterned prior to deposition of the semiconductor material thereon.

17. A process according to claim 14 wherein a layer of dielectric material is deposited over the metal layer prior to the deposition of the semiconductor material.

18. A process according to claim 17 wherein the dielectric layer comprises silicon nitride.

19. A process according to claim 1 wherein the dielectric layer is deposited by plasma enhanced chemical vapor deposition.

20. A process according to claim 1 wherein the semiconductor material comprises amorphous silicon.

21. A process according to claim 20 wherein the semiconductor material is deposited by plasma enhanced chemical vapor deposition.

22. A process according to claim 20 wherein the amorphous silicon is not patterned so that it extends continuously between at least some pairs of adjacent transistors

23. A process according to claim 20 wherein the semiconductor material further comprises a layer of n-type silicon deposited over the amorphous silicon.

24. A process according to claim 23 wherein a continuous layer of the n-type silicon is deposited over the amorphous silicon, a patterned layer of metal is thereafter formed over the n-type silicon, and the resultant structure is thereafter etched to remove portions of the n-type silicon not covered by the patterned layer of metal.

25. A process according to claim 1 wherein deposition of the semiconductor material is effected on a continuous web of substrate.

Claims 26-33 (cancelled)